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Synthesis of parallel processors / ML accelerators in Polarfire SOC FPGA

Motivation and Tasks

The primary goal of this thesis is to synthesize a new parallel processor / machine learning accelerator in a Microchip PolarFire FPGA-SOC and use it to execute Machine learning models.

To perform machine learning inference, Microchip provides the VectorBlox SDK for their series of PolarFire FPGAs, enabling the synthesis of accelerators in three performance classes: V250, V500 and V1000. Additionally, other companies that manufacture FPGAs also provide their own accelerators and toolchains to perform inference.

At the beginning of the project, a survey should be performed to identify FPGA accelerator architectures that are commonly being used by companies and scholars. Out of these architectures, one should be selected and ported onto the PolarFire MPFS250TS FPGA-SOC in the PolarFire Video Kit. Ultimately, existing machine learning models should be converted and executed in the newly synthesized accelerator architecture.

The challenge lies in the fact that while theoretically such a design can be synthesized in any FPGA, in practice the transfer of an accelerator designed for the architecture and toolchain for an FPGA manufactured by (for example) Xilinx to a Microchip PolarFire series FPGA will pose unexpected hurdles.

Goals

The project is divided into the following subtasks:

1. Literature research and selection of candidate architecture
2. Implementation of accelerator architecture on PolarFire FPGA-SOC
3. Verification of architecture by performing ML inference

What we offer

- Interesting work in current research topics
- Opportunity to contribute your own ideas when designing solutions
- Intensive supervision and support

Contact

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